

# CLAIMS

**What is claimed is:**

I claim:

1. A method, comprising:

detecting a user event in a computing system, the computing system including an integrated circuit having multiple states of performance including a first state of performance, a second state of performance higher than the first state of performance, and a third state of performance higher than the second state of performance, the computing system having a power supply which includes a battery; and

directly transitioning the integrated circuit from the first state of performance to the third state of performance based upon detecting the user event.

2. The method of claim 1, wherein the user event is defined by a programming environment within which the computing system is operating.

3. The method of claim 1, wherein directly transitioning comprises transitioning without delay.

4. The method of claim 1, further comprising:

operating the integrated circuit at the third state of performance for a predefined period of time based upon thermal considerations to operate at the third state of performance without failure.



10. The apparatus of claim 7, further comprising:

frequency regulation logic to change an operating frequency of the first integrated circuit, the frequency regulation logic to receive a signal from the program.

11. The apparatus of claim 7, further comprising:

voltage regulation logic to change an operating voltage of the first integrated circuit, the voltage regulation logic to receive a signal from the program.

12. The apparatus of claim 7, wherein the instructions reside in a Basic Input Output System.

13. The apparatus of claim 7, wherein the instructions reside in an operating system.

14. The apparatus of claim 7, wherein the instructions reside in application software.

15. The apparatus of claim 7, wherein the first integrated circuit comprises a chip set.

16. The apparatus of claim 7, wherein the first integrated circuit comprises a processing unit.

17. The apparatus of claim 12, wherein the Basic Input Output System to receive a notification signal from an operating system that the user event has occurred.

18. The apparatus of claim 11, wherein the program comprises an increasing state transition algorithm discrete from a decreasing state transition algorithm.

19. The apparatus of claim 7, wherein the program to transition the first integrated circuit to a next higher state of performance based upon an occurrence of a non-user event increasing utilization of the first integrated circuit over a preset threshold.

20. A machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform operations comprising:

detecting a user event in a computing system; the computing system including an integrated circuit having multiple states of performance including a first state of performance, a second state of performance higher than the first state of performance, and a third state of performance higher than the second state of performance; and

directly transitioning the integrated circuit from the first state of performance to the third state of performance based upon detecting the user event.

21. The machine-readable medium of claim 20, further comprising instructions which, when executed by the machine, cause the machine to perform the further operations comprising:

changing an operating frequency of the integrated circuit to change the state of performance of the integrated circuit.

22. The machine-readable medium of claim 20, further comprising instructions which, when executed by the machine, cause the machine to perform the further operations comprising:

changing an operating voltage level of the integrated circuit to change the state of performance of the integrated circuit.

23. The machine-readable medium of claim 20, further comprising instructions which, when executed by the machine, cause the machine to perform the further operations comprising:

operating the integrated circuit at the third state of performance for a transient period of time period of time.

24. An apparatus, comprising:

means for detecting a user event in a computing system; the computing system including an integrated circuit having multiple states of performance including a first state of performance, a second state of performance higher than the first state of performance, and a third state of performance higher than the second state of performance; and

means for directly transitioning the integrated circuit from the first state of performance to the third state of performance based upon detecting the user event.

25. The apparatus of claim 24, further comprising:

means for changing an operating frequency of the integrated circuit to change the state of performance of the integrated circuit.

26. The apparatus of claim 24, further comprising:

means for changing an operating voltage level of the integrated circuit to change the state of performance of the integrated circuit.

27. A machine-readable medium to provide instructions, the instructions when executed by a machine, cause the machine to perform operations comprising:

detecting a user event in a computing system being powered by a battery; the computing system including an integrated circuit having multiple states of performance including a first state of performance and a highest state of performance; and

directly transitioning the integrated circuit from the first state of performance to the highest state of performance based upon detecting the user event.

28. The machine-readable medium of claim 27, further comprising instructions which, when executed by the machine, cause the machine to perform the further operations comprising:

changing the state of performance of the integrated circuit by changing an amount of processors to manage the processing load.

29. The machine-readable medium of claim 27, further comprising instructions which, when executed by the machine, cause the machine to perform the further operations comprising:

changing the state of performance of the integrated circuit by changing an operating frequency level of the integrated circuit.

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